

**ABSTRACT**

Methods and apparatus for performing formal verification of a system defined by a set of automata are useful in facilitating computing efficiencies during the verification of an incremental system design. The various embodiments permit computing efficiencies by saving information generated during a verification of the system for use in subsequent verification runs. The saved information includes calculation results pertaining to instances or elements of the system that do not require modification for the next subsequent verification.

10015053-102901  
"06201" 35051001